Broadband High Dynamic Surveillance

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***Abstract*— In Ultra Wideband (UWB) systems, received signals may have a huge power ratio. Such signals can only be processed by an expensive receiver with a very large dynamic dynamic. This manuscript presents a hybrid receiver which contains two parts (Analog and digital) and nonlinear units based on a logarithmic amplifier. The main used topologies of logarithmic amplifiers have been implemented and tested. The manuscript describes the structure of selected and approved amplifiers. Simulation results have been conducted taking into considerations two scenarios: in the first scenario of receiver, a OFDM signal has been generated and processed by our nonlinear unit to test the relationship between input and output, and the other scenario to test behavior of the system to demodulate the sum of two OFDM signals with an amplitude very large power ratio, one very small and one very large, and graphically analyzing the constellations of both signals.**

***Keywords*— Dynamic Range Compression, Logarithmic Amplifier, wideband signals**

I. INTRODUCTION

The dynamic range (DR) of a system is defined as the ratio between the smallest and largest signals that can be handled by that system. In order to digitally process our signals, the receiver should contain an Analog to Digital Convertor (ADC). The DR of a n-bits ADC is the relationship in volts between the largest value measured and the smallest voltage value that can be converted to 1 bit. In this case, the ratio is equal to the 2^n , where *n* is the number of bits of the converter. For radio communication applications, n is generally between 8 to 14 bits [10]. However this limits the dynamic range input and makes it necessary to use Automatic Gain Control (AGC) devices to adjust the level of the input signal to fit to the ADC level. It is well known that AGC can only adjust the gain of a single signal. If the received signal is UWB or it is the sum of two or more signals, then the AGC becomes useless. OFDM signals can generate similar problem because of their Power Average Peak Ratio (PAPR) which suffers from great peaks of power, and it may cause severe issues in linear amplifiers.

To receive wideband signals, mixing signals of very different amplitudes, it is necessary to have a system with a large dynamic range. That system can compress the signal to the limit of the ADC dynamic range. This nonlinear processing should be reversed at the digital side in order to receive and demodulate correctly the received signals. In our project, we decided to implement a logarithmic amplifier as a possible solution to our problem which is the demodulation of two OFDM signals with a huge difference between their respective powers. The log function applies high gain for small signals and low gains for large amplitude signals. The logarithmic amplifier was implemented and simulated using FET transistor capable of operating at high frequencies. An architecture known as the "true log amp" developed by [1] was tested for OFDM signals, as they are currently widely used in radio communications systems.

II. FUNCTION DESCRIPTION

There are several architectures of true log amplifiers, we implemented the “dual amplifier cascaded”, as it shows good results in high frequencies. This architecture was described in [1] and [2]. The log amplifier is composed by N dual-gain stages in cascaded, see figures (1) and (2). Each stage contains an unitary amplifier and another amplifier with gain “A” followed by a saturation unit with the value “V_L”. Figure (3) shows the function transfer of each stage, where θ_1 is the stage gain until the V_L. and $\theta_2 = 1$ is the gain beyond the V_L as the unit gain amplifier is not limited. The configuration of N identical cascaded stages, as shown in figure (2), can generate the transfer function presented in figure (4). This is a series of straight lines with breakpoints corresponding to the limited amplifiers which limit the signal. After N stages the straight lines become curved ones. The breakpoints are located in the logarithmic curve given by the following expression.

$$V_{\log} = \left\{ N + \frac{1}{A} + \log_{A+1}\left[\frac{AV_{in}}{V_L}\right]\right\} V_L \qquad (1)$$

Equation (1) presents a non-linear function resultant of the circuit. This kind of logarithm depends on three parameters: number of stages (N), the gain (A) and the limit voltage (V_L). The mathematical description of the logarithmic amplifier can be found in [1].

Each dual stage is composite of four amplifiers as shown in figure (5). In that figure, the circuit in the red box is an amplifier unlimited with a gain “A”, the one in the black box is an amplifier with gain 1, but limited in VL, this two circuits are equivalent to the limited amplifier presented in figure 1. The

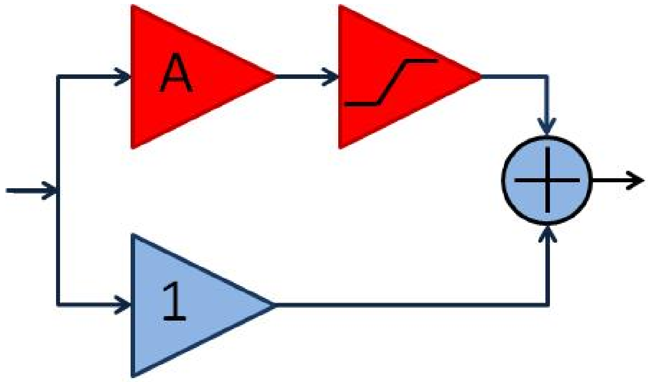

Fig. 1: Structure of dual stage

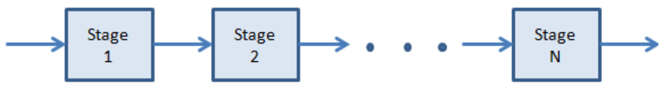

Fig. 2: Structure of the Log Amplifier

circuit in the green box is an amplifier of gain 1 unlimited. Finally, the circuit in the blue box is used to add the signals of the two amplifiers. The resistors were introduced to reduce the influence of one branch to other. However, this leads to an attenuation of 2.5, to compensate this attenuation, we introduced another amplifier presented in the brown box with the gain 2.5.

The various amplifiers of stages, were implemented using a structure of two transistors with a smaller gain in order to increase the linearity of the dual stage. In the unit gain and in the A gain amplifiers the linearity is mandatory, so it is necessary to avoid the limitation non-linearity of FET.

To create the limitation in the dual stage, two saturated amplifiers were used: The first one saturates the down side of the signal, however it is an inverting amplifier; therefore another saturated amplifier is required to make the same saturation but now in the upper side of the signal. In figure(6a), the black square represents an inverting amplifier with an unitary gain and it is polarized to saturate the signal about -0.76 and the last red square is a similar amplifier to the first square, but it saturates the signal at the same voltage; however it is polarized to saturate the signal about -0.76. This structure reached a good result waveform, as shown in the waveform of figure (6b).

According to [1] the dynamic range of this circuit is (A+1)N. The goal of our project is to receive signals with 70 dB of difference in their amplitudes, that can be done setting A=3.0, V_L=0.764 and N=6. The value of V_L fixed to a heuristic value through simulations.

III. Test System

Our circuit was tested using two tests. At first, a simple verification of the in/out relationship has been conducted. In the second test, two OFDM signals were mixed, received, processed, separated demodulated.

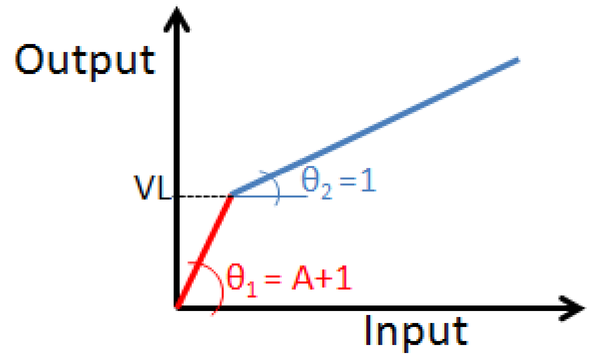

Fig. 3: Structure of dual stage

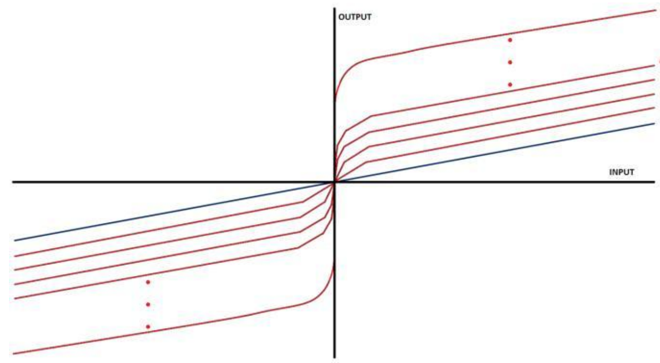

Fig. 4: Transfer function of the log amplifier

A. *Test verification of linearity*

The propose of this test is to check if the system is able to compress non linearly an OFDM signal at its analog part, reverse this nonlinearity at the digital part, then demodulate correctly the received OFDM signal. To analyze the circuit, an OFDM signal was generated in MATLAB using the steps described by [9]. The OFDM has a bandwidth of 128KHz with 256 carriers in band-base. The circuit was implemented and simulated using MICROCAP, only the real part of the signal was considered. It is worth mentioning that to cancel the effect of the non-linear unit at the analog part, the signal re-linearized based on equation (2) in the digital part of the circuit.

$$V_{a\log} = \left(\frac{V_L}{A}\right)(A+1)^{\left(\frac{V_{\log}}{V_L}-N-\left(\frac{1}{A}\right)\right)} \tag{2}$$

Figure (7) shows a comparison between the input of the system, i.e. an OFDM signal, and the output of the output signal re-linearized with the equation 2. Figure (8) shows the relationship IN x OUT. According to that figure, we can see that the non-linearity has been well inversed with gain 1. We can see in figure (7), the system of Log amp and the reconstruction function can reasonably follow the input value.

B. *Test with two OFDM signals*

The second test is to check the capacity of the system to demodulate the sum of two OFDM signals with an amplitude

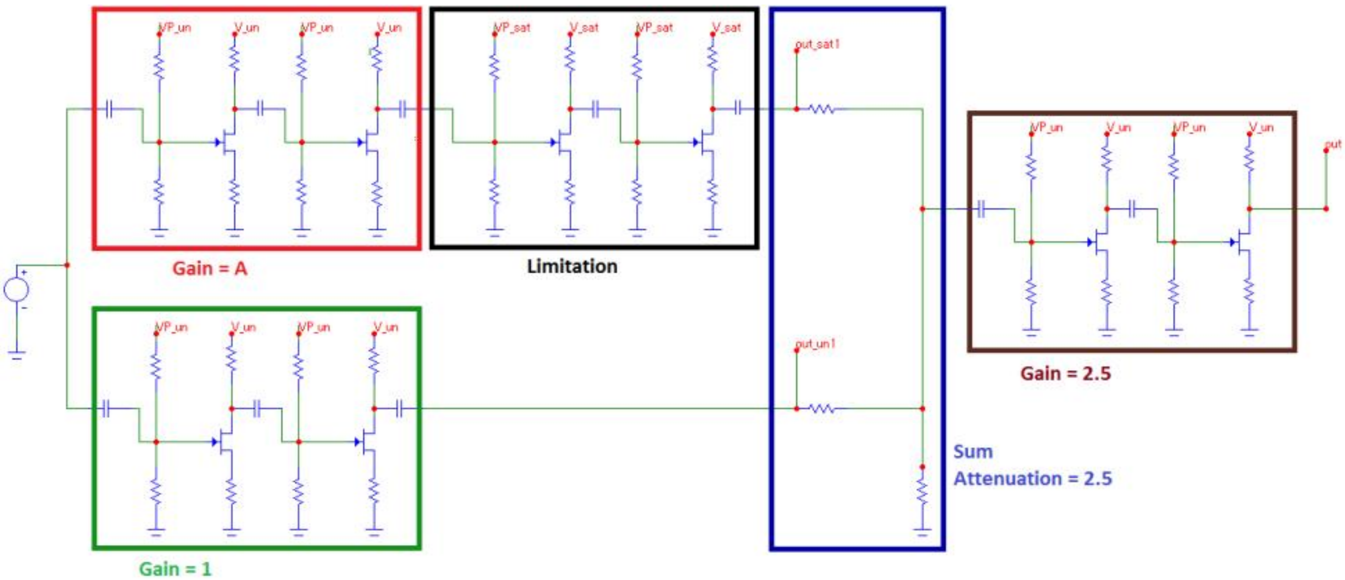

Fig. 5: Circuit of dual stage "true log amplifier"

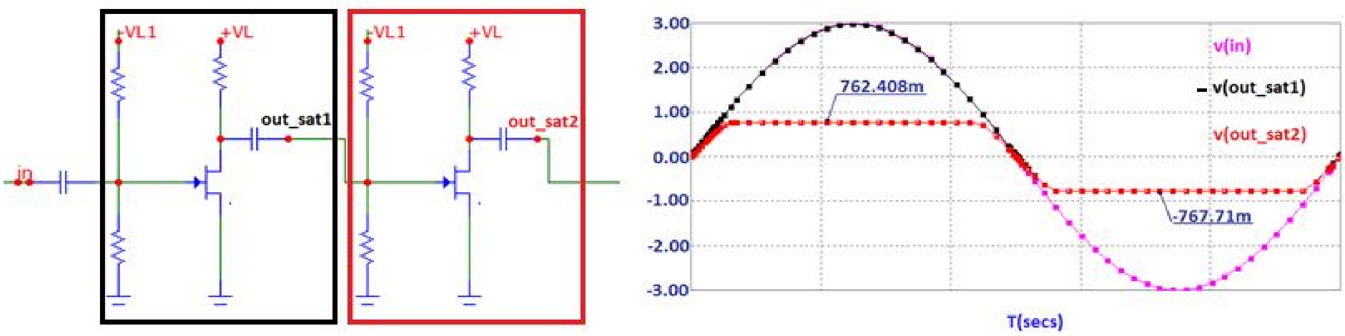

Fig. 6 : (a) Saturated Amplifier (b) Sinusoid statured

difference of 70 dB. The signals' bandwidths are supposed to be close, as seen in figure (9). The generated signals are 224µs length, each one has around 9 MHz of bandwidth. The sampling frequency is equal 5.8GHz to support the harmonics of signal in Log domain.

The OFDM demodulation was based in [9]. Each OFDM signal is an QAM16, that loads 1751 valid symbols, 297 null symbols, in 2048 carriers. The complete experiment consist of the signal generation, the simulation of Log Amplifier, ADC, the Alog and the demodulation unit, as shown in figure (10). Our goal is show that the proposed system can receive the sum of wideband signals and demodulates them separately. As a result of the previous test, we can conclude that the system formed by Amp Log plus Alog code is quite linear. The ADC has 12 bits.

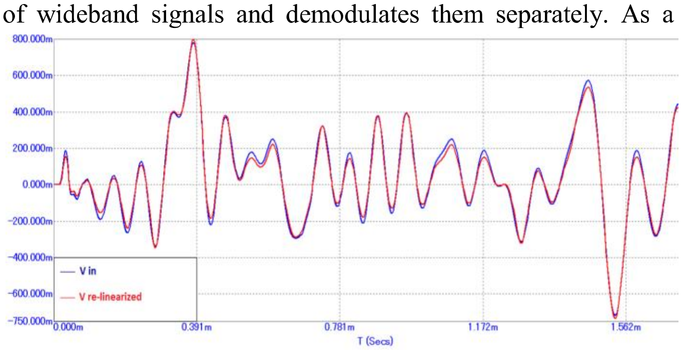

Fig.7: OFDM Signal

The block representing the Log Amplifiers is in fact a code to simulate double amplifiers dedicated to the real and the imaginary parts of complex signals. So also are the ADC, the Alog Function and filters in the same way they have two branches, one for each part of the complex signal. The filter system separates the two OFDM signals, they are 8th order, and centered in the carrier frequency of each OFDM signal and bandwidth equal to the signal.

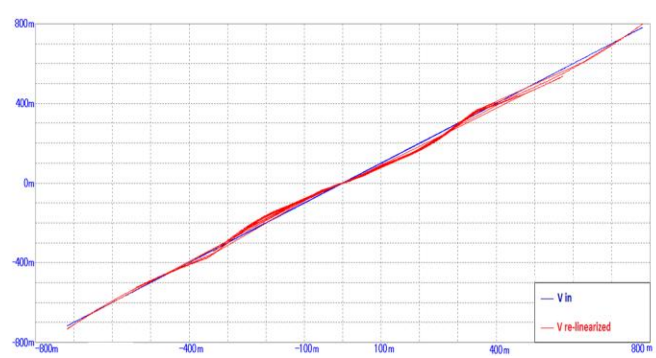

Fig.8: IN x OUT

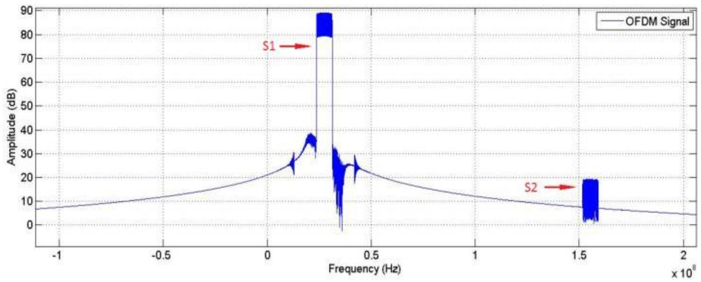

Fig.9: The spectrum of two OFDM signals

The demodulation block receives the complex signal of each portion of spectrum, to make the processing of downconverter, the downsampling, Fast Fourier Transform (FFT), the equalization, and lastly plot of constellation. The downconverter consists of bring the information back to band base, this is made by a multiplication of the complex signal by a complex exponential: $e^{-i2\pi f_c t} = \cos 2\pi f_c t - i \sin 2\pi f_c t$, where f_c stands for the carrier frequency of each signal.

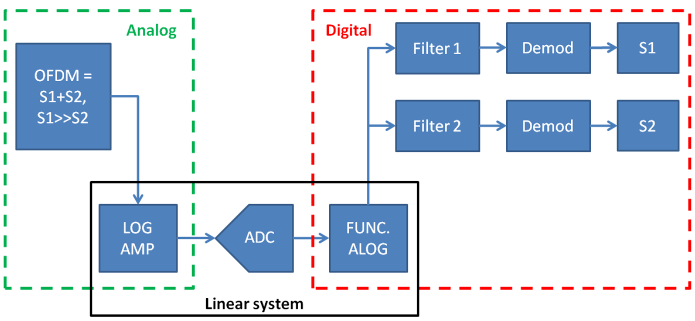

Fig.10: The Block Diagram of reception system

The generated signal has about 1.3 Mega samples, i.e. each symbol has 320 samples. The downsample removes extra samples by withdrawal of the samples followed by a low pass filter. Each symbol is transmitted over one carrier. In OFDM systems, carriers must be modulated and demodulated together by Inverse FFT (IFFT) and (FFT). The modulation by an IFFT generated orthogonal carriers. The orthogonality among carries allows the multiplexing by a set of carriers with minimum frequency spacing among each other. That eliminates the crosstalk between the carriers. Demodulation uses the FFT to bring the carriers to the previous state in order to resolve the data in each carrier.

The equalization is a processes that makes the signal amplitudes to has the same size of the modulation alphabet, QAM16, as shown by the following equation:

$$S_e = \frac{S}{S_M} * A_M \qquad (3)$$

Where S_e is the equalized signal, S_M is the maximum value of the signal, A_M is the maximum value of the Alphabet and S is the non-equalized signal.

The constellation is the representation of the symbols in a *In Phase* and *Quadrature* diagram, In figure (11), the symbols

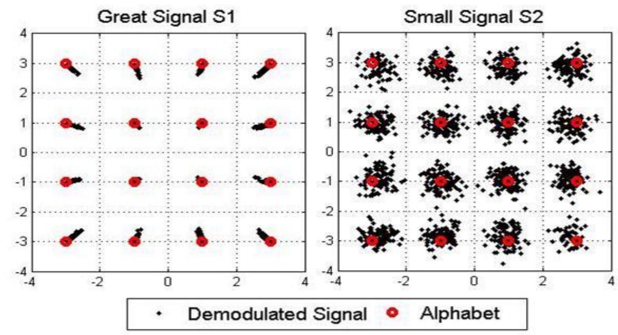

Fig.11: Constellations of Signal Re-linearized

are marked by the black dots and the alphabet of the modulation QAM16 is marked by the small red circle. We can see that the Signal to Noise Ratio is greater in S2 than S1. According to the results of figure 11, we can conclude that even the weak signal S2 is perfectly demodulated.

CONCLUSION

In order to demodulate the sum of two wideband signals with a huge difference of theirs amplitudes, we proposed a hybrid system (analog and digital parts) based on the Log Amplifier. The log amplifier shows good results in reducing the dynamic range of signals. Goods results have been observed at the output of the whole system considering two nonlinear units at the analog and the digital parts.

Our future works will upgrade the circuit to make it low noise amplifiers and introducing impedance matching to make the amplifier useful in the real applications.

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